Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of http://www.nxp.com, http://www.philips.com/ or http://www.semiconductors.philips.com/, use **http://www.nexperia.com**

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use **salesaddresses@nexperia.com** (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:
- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved
Should be replaced with:
- **© Nexperia B.V. (year). All rights reserved**.

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

PMN50XP

P-channel TrenchMOS extremely low level FET

Rev. 02 — 2 October 2007 Product data sheet

1. Product profile

1.1 General description

Extremely low level P-channel enhancement mode Field-Effect Transistor (FET) in a plastic package. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features

- Low on-state losses
- Low threshold voltage

1.3 Applications

- Battery management
- Load Switching
- Battery powered portable equipment
- Low power DC to DC converters

1.4 Quick reference data

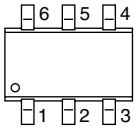
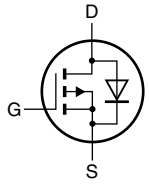
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C	-	-	-20	V
I_D	drain current	V_{GS} = -4.5 V; T_{sp} = 25 °C; see Figure 1 and 3	-	-	-4.8	A
Dynamic characteristics						
Q_{GD}	gate-drain charge	V_{GS} = -4.5 V; I_D = -4.7 A; V_{DS} = -10 V; T_j = 25 °C; see Figure 9 and 10	-	1.3	-	nC
Static characteristics						
R_{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -2.8 A; T_j = 25 °C; see Figure 7 and 8	-	48	60	mΩ

founded by Philips

2. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic Symbol
1	D	drain		
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		

003aaa671

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMN50XP	TSOP6	plastic surface-mounted package (TSOP6); 6 leads	SOT457

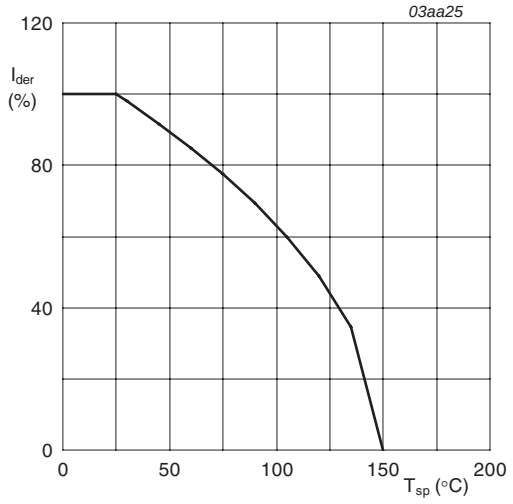
4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

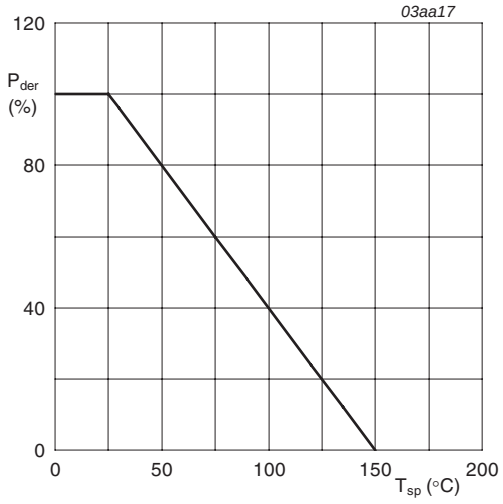
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C	-	-20	V
V_{DGR}	drain-gate voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C; R_{GS} = 20 kΩ	-	-20	V
V_{GS}	gate-source voltage		-12	12	V
I_D	drain current	T_{sp} = 25 °C; V_{GS} = -4.5 V; see Figure 1 and 3	-	-4.8	A
		T_{sp} = 100 °C; V_{GS} = -4.5 V	-	-3	A
I_{DM}	peak drain current	T_{sp} = 25 °C; t_p < 10 μs; pulsed; see Figure 3	-	-19.4	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; see Figure 2	-	2.2	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
Source-drain diode					
I_S	source current	T_{sp} = 25 °C	-	-1.9	A
I_{SM}	peak source current	T_{sp} = 25 °C; $t_p \leq 10$ μs; pulsed	-	-7.5	A

© NXP B.V. 2007. All rights reserved.



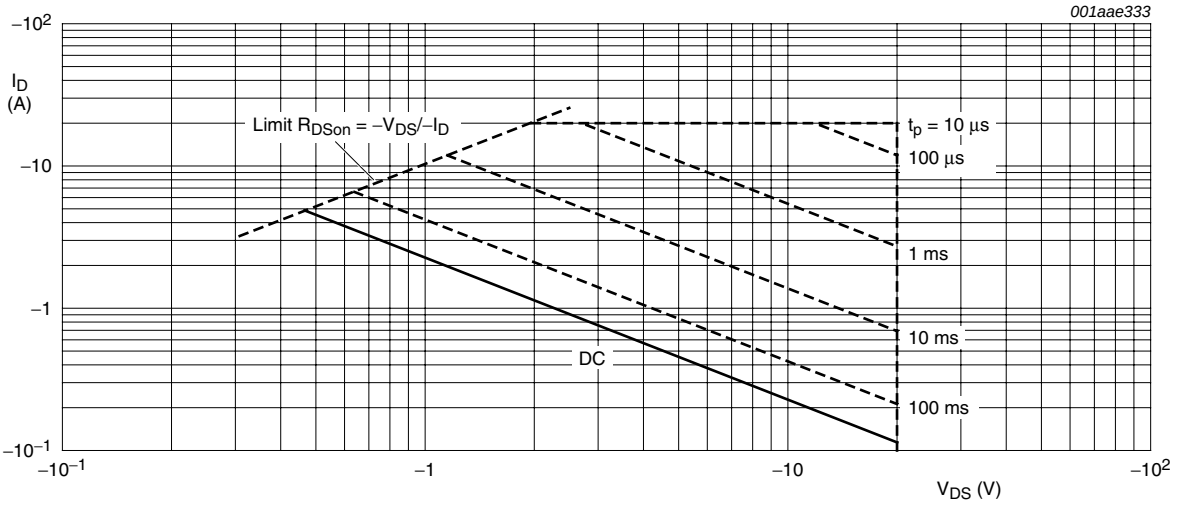
$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

Fig 1. Normalized continuous drain current as a function of solder point temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature



T_{sp} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

© NXP B.V. 2007. All rights reserved.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 4	-	-	55	K/W

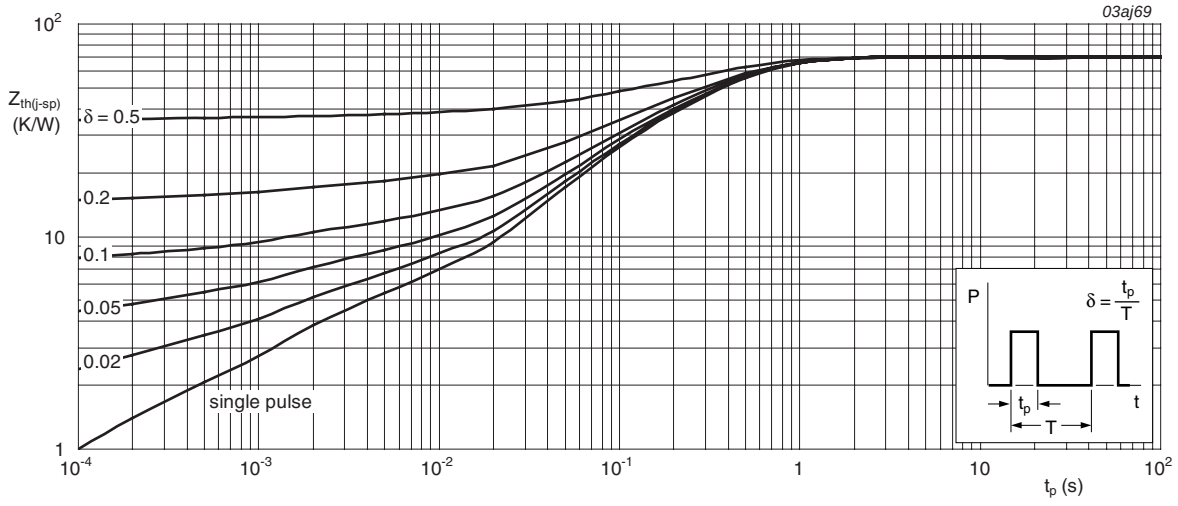


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 6. Characteristics

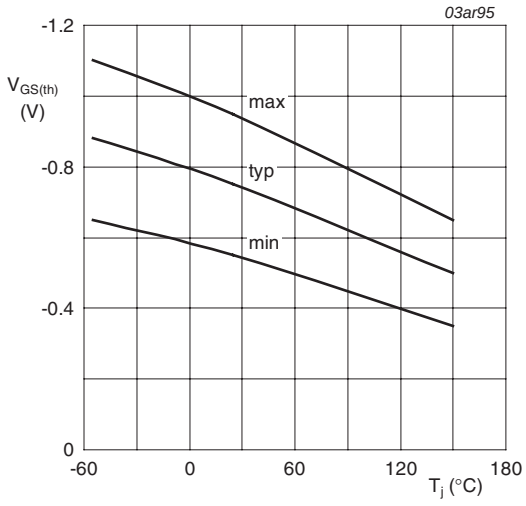
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = -250 µA; V_{GS} = 0 V; T_j = 25 °C	-20	-	-	V
		I_D = -250 µA; V_{GS} = 0 V; T_j = -55 °C	-18	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = -0.25 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 5 and 6	-0.55	-0.75	-0.95	V
		I_D = -0.25 mA; V_{DS} = V_{GS}; T_j = 150 °C; see Figure 5 and 6	-0.35	-	-	V
		I_D = -0.25 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 5 and 6	-	-	-1.1	V
I_{DSS}	drain leakage current	V_{DS} = -20 V; V_{GS} = 0 V; T_j = 25 °C	-	-	-1	µA
		V_{DS} = -20 V; V_{GS} = 0 V; T_j = 70 °C	-	-	-5	µA

© NXP B.V. 2007. All rights reserved.

Table 6. Characteristics *…continued*

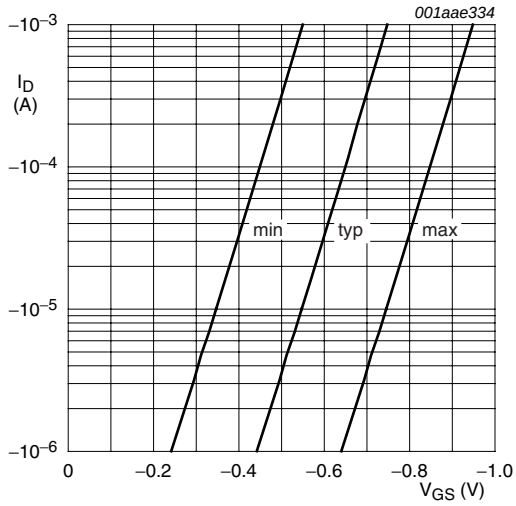
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{GSS}	gate leakage current	$V_{GS} \leq 12$ V; $V_{DS} = 0$ V; $T_j = 25$ °C	-	-10	-100	nA
		$V_{GS} \geq 12$ V; $V_{DS} = 0$ V; $T_j = 25$ °C	-	-10	-100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5$ V; $I_D = -2.8$ A; $T_j = 25$ °C; see Figure 7 and 8	-	48	60	mΩ
		$V_{GS} = -4.5$ V; $I_D = -2.8$ A; $T_j = 150$ °C; see Figure 7 and 8	-	77	96	mΩ
		$V_{GS} = -2.5$ V; $I_D = -2.3$ A; $T_j = 25$ °C; see Figure 7 and 8	-	65	80	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = -4.7$ A; $V_{DS} = -10$ V; $V_{GS} = -4.5$ V; $T_j = 25$ °C; see Figure 9 and 10	-	10	-	nC
Q_{GS}	gate-source charge	$I_D = -4.7$ A; $V_{DS} = -10$ V; $V_{GS} = -4.5$ V; $T_j = 25$ °C; see Figure 9 and 10	-	2.2	-	nC
Q_{GD}	gate-drain charge	$I_D = -4.7$ A; $V_{DS} = -10$ V; $V_{GS} = -4.5$ V; $T_j = 25$ °C; see Figure 9 and 10	-	1.3	-	nC
C_{iss}	input capacitance	$V_{DS} = -20$ V; $V_{GS} = 0$ V; f = 1 MHz; $T_j = 25$ °C; see Figure 11	-	1020	-	pF
C_{oss}	output capacitance	$V_{GS} = 0$ V; $V_{DS} = -20$ V; f = 1 MHz; $T_j = 25$ °C; see Figure 11	-	140	-	pF
C_{rss}	reverse transfer capacitance	$V_{DS} = -20$ V; $V_{GS} = 0$ V; f = 1 MHz; $T_j = 25$ °C; see Figure 11	-	100	-	pF
$t_{d(on)}$	turn-on delay time	$R_{G(ext)} = 6\ \Omega$; $R_L = 10\ \Omega$; $V_{DS} = -10$ V; $V_{GS} = -4.5$ V; $T_j = 25$ °C	-	8.5	-	ns
t_r	rise time	$R_{G(ext)} = 6\ \Omega$; $R_L = 10\ \Omega$; $V_{DS} = -10$ V; $V_{GS} = -4.5$ V; $T_j = 25$ °C	-	7.5	-	ns
$t_{d(off)}$	turn-off delay time	$V_{DS} = -10$ V; $R_L = 10\ \Omega$; $V_{GS} = -4.5$ V; $R_{G(ext)} = 6\ \Omega$; $T_j = 25$ °C	-	82	-	ns
t_f	fall time	$R_{G(ext)} = 6\ \Omega$; $R_L = 6\ \Omega$; $V_{DS} = -10$ V; $V_{GS} = -4.5$ V; $T_j = 25$ °C	-	35	-	ns
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = -10$ V; $I_D = -4.7$ A; $T_j = 25$ °C; see Figure 9 and 10	-	-1.6	-	V
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = -1.7$ A; $V_{GS} = 0$ V; $T_j = 25$ °C	-	-0.77	-1.2	V
t_{rr}	reverse recovery time	$I_S = 3.5$ A; $dI_S/dt = -100$ A/µs; $V_{GS} = 0$ V; $V_{DS} = 20$ V; $T_j = 25$ °C	-	-	-	ns

© NXP B.V. 2007. All rights reserved.



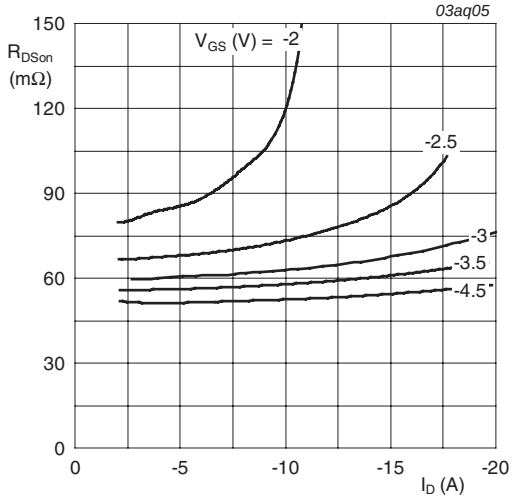
$I_D = -0.25\ mA; V_{DS} = V_{GS}$

Fig 5. Gate-source threshold voltage as a function of junction temperature



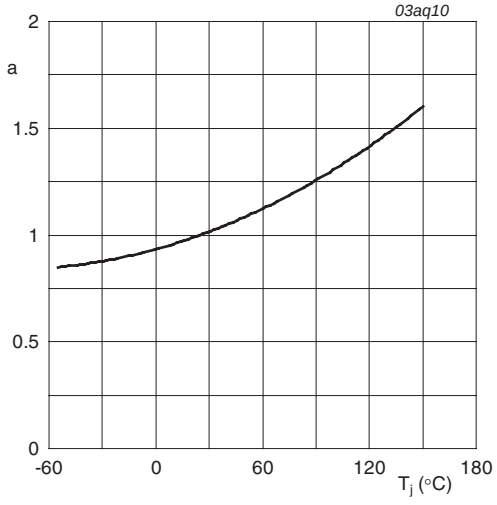
$T_j = 25\ °C; V_{DS} = -5\ V$

Fig 6. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25\ °C$

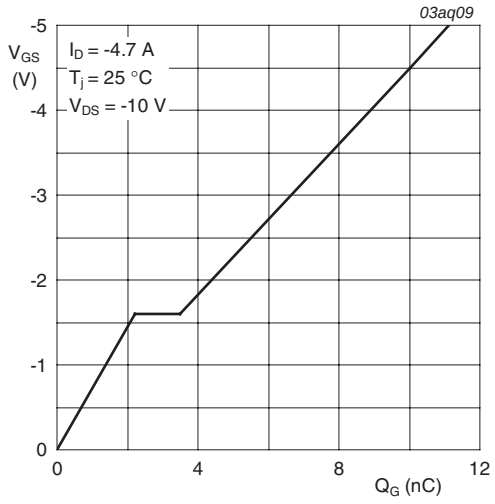
Fig 7. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature

© NXP B.V. 2007. All rights reserved.



$I_D = -4.7\ A; T_j = 25\ °C; V_{DS} = -10\ V$

Fig 9. Gate-source voltage as a function of gate charge; typical values

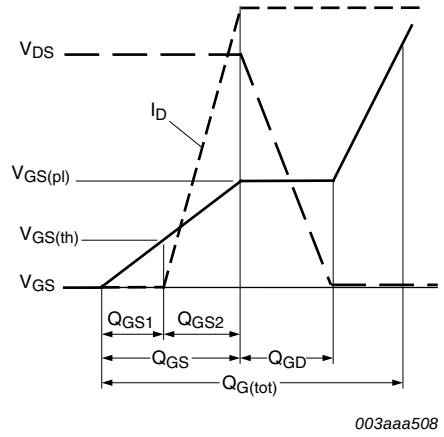
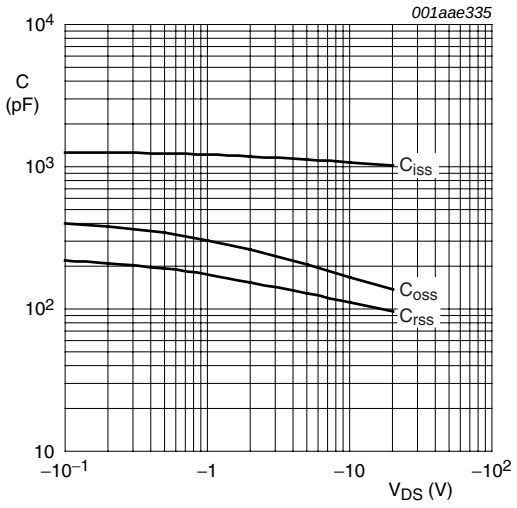


Fig 10. Gate charge waveform definitions



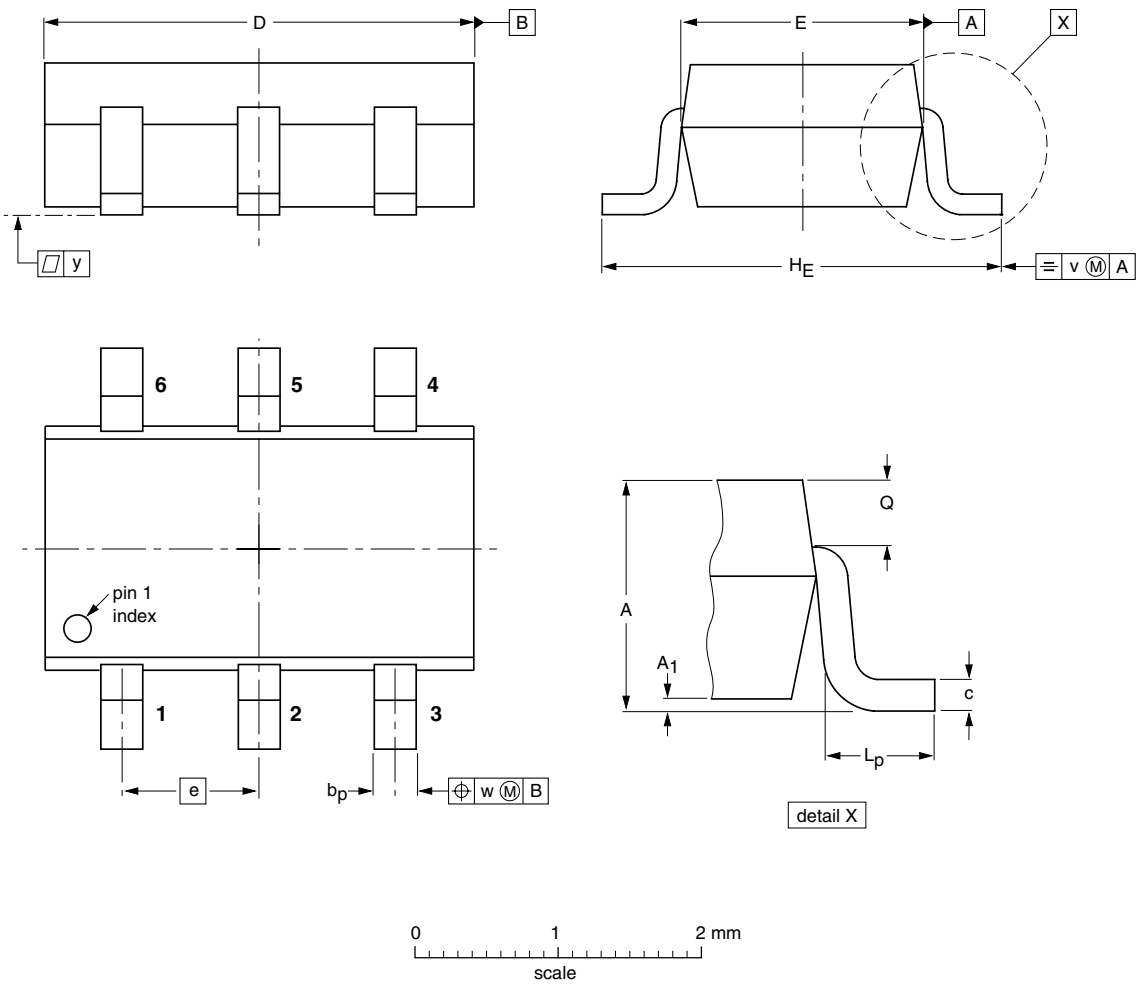
$V_{GS} = 0\ V;\ f = 1\ MHz$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

© NXP B.V. 2007. All rights reserved.

7. Package outline

Plastic surface-mounted package (TSOP6); 6 leads **SOT457**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT457			SC-74			~~05-11-07~~ 06-03-16

Fig 12. Package outline SOT457 (TSOP6)

© NXP B.V. 2007. All rights reserved.

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMN50XP_2	20071002	Product data sheet	-	PMN50XP_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the company name where appropriate.			
PMN50XP_1	20060123	Product data sheet	-	-

© NXP B.V. 2007. All rights reserved.

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

9.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

9.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

9.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

TrenchMOS — is a trademark of NXP B.V.

10. Contact information

For additional information, please visit: **http://www.nxp.com**

For sales office addresses, send an email to: **salesaddresses@nxp.com**

© NXP B.V. 2007. All rights reserved.

11. Contents

1	**Product profile**	**1**
1.1	General description	1
1.2	Features	1
1.3	Applications	1
1.4	Quick reference data	1
2	**Pinning information**	**2**
3	**Ordering information**	**2**
4	**Limiting values**	**2**
5	**Thermal characteristics**	**4**
6	**Characteristics**	**4**
7	**Package outline**	**8**
8	**Revision history**	**9**
9	**Legal information**	**10**
9.1	Data sheet status	10
9.2	Definitions	10
9.3	Disclaimers	10
9.4	Trademarks	10
10	**Contact information**	**10**
11	**Contents**	**11**

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2007. **All rights reserved.**

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 2 October 2007
Document identifier: PMN50XP_2

founded by

PHILIPS